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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,138	07/25/2003	Ryoji Suzuki	09792909-5649	3927

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
10/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/627,138	SUZUKI ET AL.	
	Examiner	Art Unit	
	NHAN T. TRAN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/11/2009 and 7/23/2009 has been entered.

Response to Arguments

2. Applicant's arguments filed 7/23/2009 have been fully considered but they are not persuasive.

The Applicant asserts that the combined teaching of Nishizawa and Arakawa does not teach or suggest a pixel unit having a selection circuit between a horizontal reset line and a reset element which is configured to provide a reset signal to the reset element or a selection signal to a selection element. Instead, Nishizawa discloses two switching transistors, where one transistor transfers a photoelectric converting voltage from a yellow color pixel to a terminal and the other transistor transfers a photoelectric converting voltage from a green color pixel to a second terminal (remarks, page 3).

In response, the Examiner understands the Applicant's arguments but respectfully disagrees.

It is seen that the claim is written broad enough to read on the disclosure of Nishizawa and Arakawa. As shown by Fig. 1 of Nishizawa, the selection circuit (e.g., circuit of transistors Q10 and Q11) is located between a horizontal reset line (reset line VRP that runs from Q16-Q18, col. 3, lines 45-52) and the reset element (Q1, Q4 or Q7, col. 3, lines 3-20). In view of the above, the claim limitations are met by the combined teaching of Nishizawa and Arakawa.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishizawa et al. (US 5,122,881) in view of Arakawa (US 6,031,571).

Regarding claim 27, Nishizawa discloses a solid-state image sensor (Fig. 1) comprising: (a) a plurality of unit pixels (Fig. 1) with each unit pixel having (i) a photoelectric conversion element (D1) which converts incident light into an electric signal charge and stores the electric signal charge obtained through such photoelectric conversion; (ii) an amplifying element (Q2) connected to the photoelectric conversion element and which is effective to amplify the electric signal charge stored in said photoelectric conversion element into an electric signal; (iii) a reset element (Q1)

connected between the photoelectric conversion element (D1) and a power supply (PDRV) and which is effective to reset said electric signal charge; (iv) a selection element (Q3) between the amplifying element and a signal line (column output VI) (see Fig. 1 and col. 2, line 55 - col. 3, line 44);

(v) a selection circuit (the circuit of transistors Q10 and Q11) between a horizontal reset line (VRP line that runs from Q16-Q18, col. 3, lines 45-52) and the reset element (Q1, Q4 or Q7) which is configured to provide a reset signal (by turning on transistor Q10) to the reset element and a selection signal (by turning on transistor Q11) to the selection element (col. 3, line 63 - col. 4, line 28).

Nishizawa is silent as to the reset element is a depletion mode transistor, and the reset gate of said depletion mode transistor is a transverse overflow barrier effective to dump excess charge to the power supply. However, it is well recognized by Arakawa that a reset element can be implemented by a depletion mode transistor (col. 1, lines 49-54) and the reset gate of the depletion mode transistor is a transverse overflow barrier (see Arakawa, Fig. 2 & 4 in which the reset gate 3 creates an overflow transverse barrier by applying different voltages ¢1 and ¢2).

Therefore, it would have been obvious to one of ordinary skill in the art to configure the reset element in Nishizawa to be a depletion mode transistor and the reset gate of the depletion mode transistor is a transverse overflow barrier for reducing power consumption for the image sensor as suggested by Arakawa in col. 3, lines 35-39.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NHAN T. TRAN whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NHAN T TRAN/
Primary Examiner, Art Unit 2622